First Experimental Demonstration of Ge 3D FinFET CMOS Circuits

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I. Abstract

We report the first experimental demonstration of Ge 3D CMOS circuits, based on the recessed fin structure. Both n-FinFETs and p-FinFETs with channel length (L_{ch}) from 200 to 20 nm and fin width (W_{Fin}) from 60 to 10 nm are realized on a Ge-on-insulator (GeOI) substrate. The Ge FinFETs show superior gate electrostatic control over planar devices and sub-threshold slope (SS) as low as 93 and 73 mV/dec are obtained on n- and p-FETs, respectively. Combining the n- and p- type 3D devices together, the FinFET CMOS inverters have high voltage gain up to 34 V/V at V_{DD} of 1.4 V, delivering more than 200% improvement over the planar ones at the same L_{ch} of 200 nm. Scalability studies are also carried out for both types of FinFETs in terms of L_{ch} and W_{Fin}.

II. Introduction

Recently, Ge CMOS circuits have been experimentally demonstrated on GeOI [1] or poly-Ge substrate [2], showing the promise of Ge CMOS for post-Si technology node. However, the device characteristics such as SS, DIBL and L_{ch} scaling metrics of the planar Ge recessed channel MOSFETs [3] are still greatly limited by the planar structure, suffering from relatively severe short channel effects (SCEs). Various 3D structures such as: tri-gate fin [4-5], Ω-gate [6] and gate all around (GAA) nanowire [7] have been widely applied to Ge [8-14] or III-V compounds [15] to enhance the gate electrostatics, demonstrating the scaling of device down to sub-20 nm. However, to our best knowledge, there's no CMOS circuit level work reported on Ge 3D transistors [13-17].

In this paper, we successfully integrate the 3D fin structure into the recessed channel, building up the first Ge 3D FinFET CMOS circuits. The introduction of 3D structure has allowed the demonstration of decent SSs of 93 and 73 mV/dec on 200 nm L_{ch} for n- and p- type devices and high voltage gains up to 34 V/V for CMOS inverters, providing more than 200% improvement over the planar ones. L_{ch}, W_{Fin} and doping concentration dependence of device characteristics are also studied in great details.

III. Experiment

Fig. 1(a) summarizes the fabrication processes of the Ge recessed FinFET CMOS and Fig. 1(b) gives the CMOS inverter schematic, with the recessed fin highlighted, which is further enlarged in Fig. 1(c) for a better illustration with the doping density plotted as the color map. For balanced device performance, 4 recessed fins are employed for nFETs and 5 for pFETs. The experiment started with a GeOI wafer grown by the Smartcut™ technology from Soitec™. After a standard cleaning, the device isolation was carried out by dry etching. Next, the samples were selectively P and BF_2 implanted consequently, which were activated by rapid thermal annealing (RTA), respectively. Note that a split condition with low and shallow doping was used in the P implantation to study the doping density dependence. Then, an optimized *common* SF_6 dry etching was used to form the recessed channel, followed by another *common* dry etching process to define the fins in the channel. The fin dry etching is carefully calibrated to get a near vertical side wall surface with high aspect ratio. After a surface wet clean, 1 nm Al_2O_3 capping layer was first deposited and then the post-oxidation was performed as the interface passivation, continued by a *common* 8 nm ALD Al_2O_3 gate dielectric deposition. After a post deposition annealing (PDA) in forming gas ambient, *common* recessed S/D etching was conducted, with Ni deposited as the *common* contact metal, followed by an ohmic annealing. Finally, the *common* gate metal was formed by Ni/Au for both nFETs and pFETs and devices were connected for the logic gates.

IV. Results and Discussion

The fabricated devices have L_{ch} from 200 to 20 nm, W_{Fin} from 60 to 10 nm fin height (H_{Fin}) of 30 nm and EOT of around 4.5 nm, considering both Al_2O_3 and GeO_x. Fig. 2(a) shows a FinFET CMOS inverter under SEM, with n-FinFET and p-FinFET marked and the gate area of p-FinFET is enlarged in Fig. 2(b), showing 5 fin in parallel as the conducting channel. To better illustrate the recessed fins, testing structure without the gate metal is shown in Fig. 2(c) and the small notches in the middle of fins are the recessed fins. Thanks to the well-calibrated dry etching process, fins as narrow as 10 nm and with high aspect ratio of 18 can be realized, as shown in Fig. 3.

Fig. 4(a) gives the transfer curves of a typical Ge p-FinFET with L_{ch} = 200 nm, W_{Fin} = 10 nm and V_{gs} from -0.6 to -2 V at various V_{ds}, showing a threshold voltage (V_{TH}) of -1.1V, I_{max} of 366 mA/mm and ignorable DIBL. The trans-conductance (g_m) versus V_{gs} is given in Fig. 4(b) and a decent g_{max} of 555 mS/mm is achieved at V_{ds} of -1 V. A Ge n-FinFET with identical geometry features as the p-FinFET in Fig. 4 is given in Fig. 5, showing a large I_{ON}/I_{OFF} ratio of more than 10^5, I_{max} of 200 mA/mm, g_{max} of 354 mS/mm and a low SS of 93 mV/dec, which is the one of the lowest values reported on Ge nFETs in such scaled L_{ch} [18-23]. For Ge p-FinFETs, the lowest SS value obtained in this work is 73 mV/dec, as shown in Fig. 6, corresponding to a mid-gap interface trap density of 10^{12} $cm^{-2}\cdot eV^{-1}$, indicating a decent oxide-semiconductor interface after the fabrication process.

Fig. 7(a) shows the V_{TH} scaling metrics of Ge p-FinFETs and V_{TH} gets smaller with shrinking channel length due to severer SCEs. It's also found that smaller W_{Fin} provides larger V_{TH}, indicating better gate electrostatic control. Fig. 7(b) gives the dependence of DIBL on L_{ch}, benchmarked with planar Ge pFETs of 25 nm channel thickness (T_{ch}) [3]. The 3D fin structures have much smaller DIBL especially in short channel case (L_{ch} < 100 nm) and DIBL is reduced with smaller W_{Fin}. Fig. 7(c) shows the SS versus L_{ch} at low V_{ds} of -0.05 V, including the same set of planar pFETs. The SS of FinFETs remains unchanged till L_{ch} < 50 nm and the 3D structure provides over 25% SS reduction compared with the planar ones. Improving the interface quality, reducing the EOT of gate dielectric and employing GAA structure with a better gate control, are needed to further reduce the SS. Fig. 7(c) shows the g_{max} versus L_{ch} at high V_{ds} of -1 V and g_{max} increases with decreasing L_{ch}. In terms of the W_{Fin} dependence, for W_{Fin} = 20, 30 and 40 nm, there's almost no dependence of g_{max} on W_{Fin}. However, for devices with W_{Fin} = 10 nm, it shows about 40% g_{max} enhancement over others with a larger W_{Fin}, This is related with the volume inversion effect when the Ge fin width is reduced to 10 nm or less. The similar effect has been widely reported in Si [24-26] and III-V [27] 3D MOSFETs already.

Fig. 8(a) gives the V_{TH} scaling metrics of Ge n-FinFETs with different doping densities. A clear trend of V_{TH} roll-off is confirmed. Different from conventional inversion-mode devices, the transistors here are accumulation mode devices and the source/drain and the channel are all doped with P ions for the n-FinFETs. Higher doping concentration requires more negative gate bias to deplete the channel, thus turn off the device. Therefore, V_{TH} gets smaller with higher doping density. Fig. 8(b) shows the DIBL versus L_{ch} of Ge n-FinFETs, compared with planar Ge nFETs of 25 nm T_{ch} [3]. Similar to that of Ge pFETs, 3D structure provides much smaller DIBL. Fig. 9(a) gives L_{ch} dependence of SS of Ge nFinFETs at V_{ds} of 0.05 V, including the same set of planar nFETs. The FinFETs offer more than 40% SS reduction. The W_{Fin} dependence of SS is given in Fig. 9(b) and smaller fin size gets better SS, due to better gate electrostatics.

Fig. 10 provides the V_{IN}-V_{OUT} curves of a 200 nm L_{ch} and 10 nm W_{Fin} FinFET CMOS inverter, showing a very steep voltage transition. The voltage gain is further extracted, as given in Fig. 11 and the max voltage gain is about 34 V/V at V_{DD} of 1.4 V. Fig. 12 compares the Ge FinFET CMOS inverter in this work with Ge planar CMOS inverter reported earlier [1] at the same L_{ch} of 200 nm, showing more than 200% voltage gain improvement by employing the 3D tri-gate fin structure.

V. Conclusion

We present the first experimental demonstration of Ge 3D FinFET CMOS circuits. Thanks to the better gate control from the 3D fin structure, both SS and DIBL are improved significantly and SS as low as 93 and 73 mV/dec are obtained for n-FinFETs and p-FinFETs, respectively. Ge FinFET CMOS inverters with high voltage gain up to 34 V/V are also demonstrated.

VI. Reference

[1] H. Wu, et al., *IEDM* 2014, p.227. [2] Y. Kamata, et al., *SSDM* 2014, p.668. [3] H. Wu, et al., *IEDM* 2014, p.426. [4] J. Mitard, et al., *VLSI* 2009, p.82. [5] B. Duriez, et al., *IEDM* 2013, p.522. [6] B. Liu, et al., *EDL*, p.1336, 2012. [7] W Chern, et al., *IEDM* 2012, p.387. [8] J. Mitard, et al., *VLSI* 2009, p.82. [9] R. Zhang, et al., *VLSI* 2011, p.56. [10] C. Lee, et al., *IEDM* 2009, p.324. [11] T. Krishnamohan, et al., *TED*, p.990, 2006. [12] R. Pillarisetty, *Nature*, p.324, 2011. [13] S. Takagi, et al., *IEDM* 2012, p.505. [14] A. Tourimi, et al., *IEDM* 2011, p.646. [15] J. del. Alamo, *Nature*, p.317, 2011. [16] H. Sunamura, et al., *VLSI* 2014, p.180. [17] C. Chung, et al., *IEDM* 2012, p.383. [18] X. Gong, et al., *IEDM*, 2014, p.231. [19] M. J. H. van Dal., et al., *IEDM* 2014, p.235. [20] I. Wong, et al., *IEDM*, 2014, p.239. [21] J. Mitard, et al., *IEDM*, 2014, p.418. [22] K. Usuda, et al., *IEDM* 2014, p.422. [23] J. Park, et al., IEDM 2008, p.389. [24] H. Majima, et al., *IEDM* 2001, p.733 [25] S. Suk, et al., *IEDM*, 2007, p.891. [26] S. Bangsaruntip, et al., *IEDM* 2009, p.297. [27] J. Gu, *EDL*, p.217, 2012.

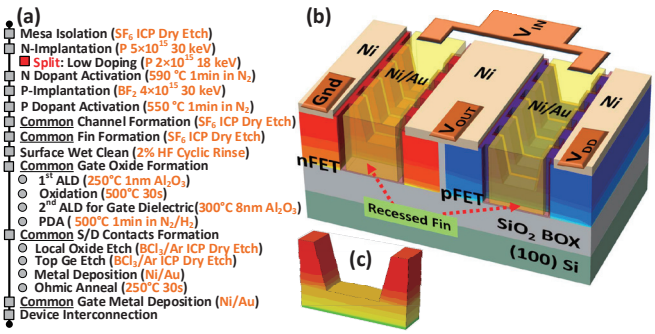

Fig. 1 (a) Key processes in the fabrication of the Ge FinFET CMOS. (b) Device schematic of a Ge FinFET CMOS inverter. Note that 4 recessed fins were employed in the n-FinFETs and 5 fins for the p-FinFETs for balanced performance. (c) Illustration of the recessed fin structure.

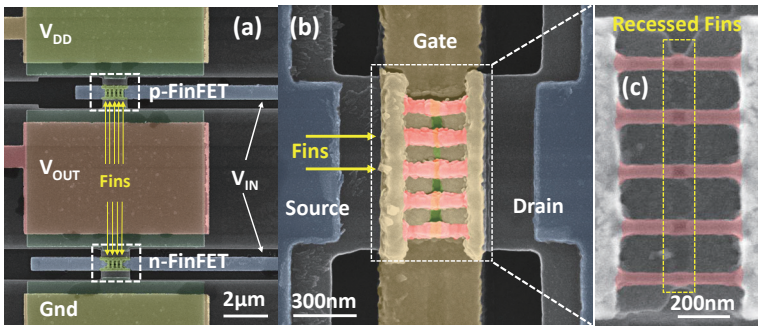

Fig. 2 (a) Top down SEM image of a fabricated Ge FinFET CMOS inverter. The fin structure in the channel could be clearly observed. (b) The channel area of a fabricated p-FinFET with 5 conducting fins. (c) Zoom-in view of the fin area in (b) with the gate metal removed. The recessed fin region is highlighted.

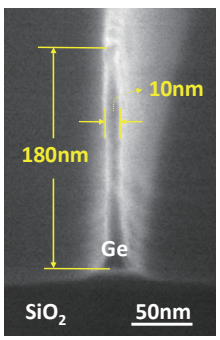

Fig. 3 One of the narrowest fin structures with W_{Fin} = 10 nm and aspect ratio of 18.

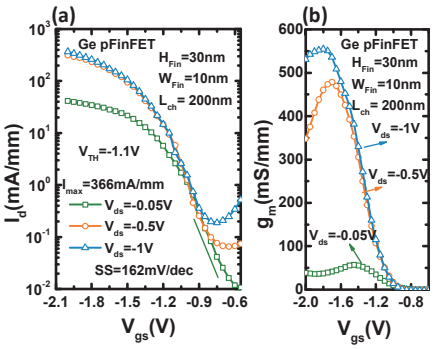

Fig. 4 (a) Transfer curves of a 200 nm L_{ch} Ge p-FinFET with V_{gs} from -0.6 to -2 V at various V_{ds} bias. (b) The g_m versus V_{gs} of the same device in (a). A decent g_{max} of 555 mS/mm is obtained.

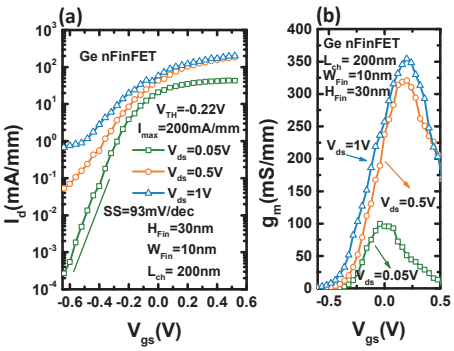

Fig. 5 (a) Transfer curves of a 200 nm L_{ch} Ge n-FinFET with V_{gs} from -0.6 to 0.5 V at various V_{ds} bias. Low SS of 93 mV/dec is obtained. (b) The g_m versus V_{gs} of the same device in (a).

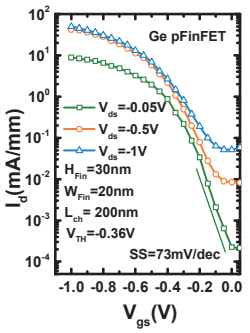

Fig. 6 Transfer curves of a Ge p-FinFET with the lowest SS of 73mV/dec.

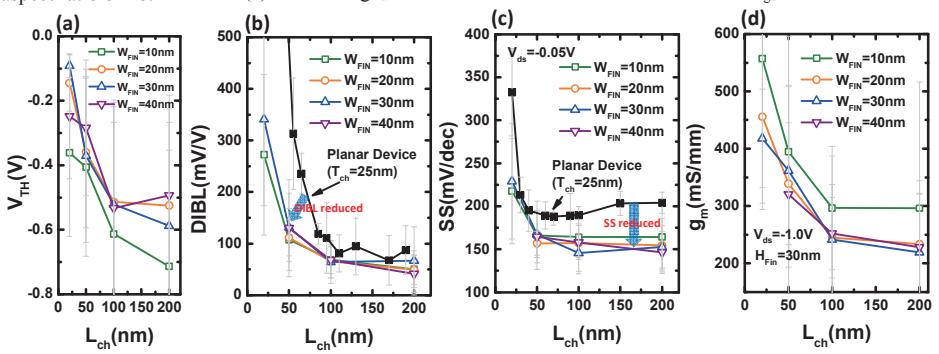

Fig. 7 Scaling metrics of Ge p-FinFETs with W_{Fin} of 10, 20, 30 and 40 nm. Scale bars give the standard deviations of data points of more than 5 devices measured. (a) L_{ch} dependence of the V_{TH}. (b) DIBL versus L_{ch}. Planar pFETs with T_{ch} of 25 nm are benchmarked. (c) L_{ch} dependence of SS at low V_{ds} of -0.05V, SSs of the same set of planar pFETs in (b) are also compared. (d) L_{ch} dependence of g_{max} at V_{ds} of 1 V.

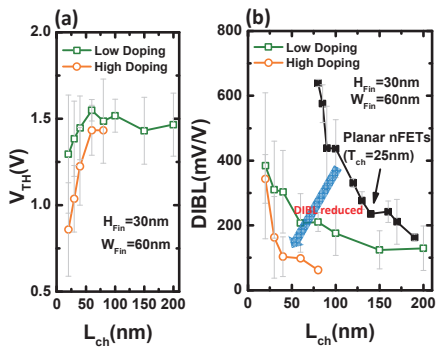

Fig. 8 L_{ch} dependence of 60 nm W_{Fin} Ge n-FinFETs with low and high doping. (a) V_{TH} metrics. (b) DIBL metrics, benchmarked with planar nFETs of 25nm T_{ch}.

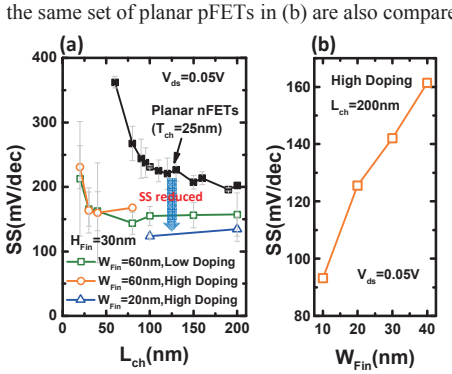

Fig. 9 (a) SS scaling metrics of 60 and 20 nm W_{Fin} Ge nFinFETs with low and high doping. Planar nFETs are also compared. (b) Dependence of SS on W_{Fin}.

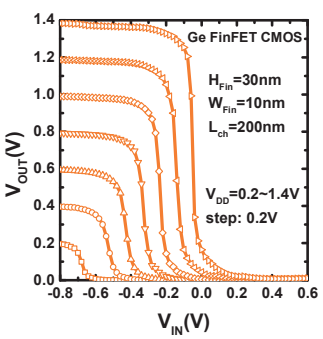

Fig. 10 V_{OUT} versus V_{IN} of a 200 nm L_{ch} and 10 nm W_{Fin} FinFET CMOS inverter at various V_{DD}.

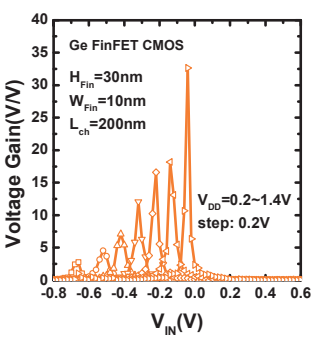

Fig. 11 Voltage gain versus V_{IN} of the same FinFET CMOS inverter in Fig. 10.

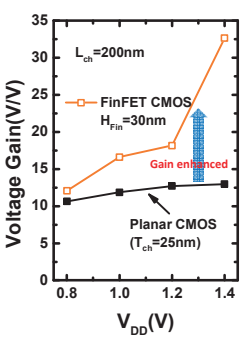

Fig. 12 Benchmark of voltage gain of 3D and planar CMOS inverter with L_{ch} of 200 nm.